REMARKS

Claims 1-17 are pending in the Application. Claims 1, 6, and 11 are independent. Claims 1 and 6 have been amended.

Claim Objections

The Patent Office objected to Claims 1 and 6 because of the following informalities: line 11 of Claim 1 and line 12 of Claim 6 replaces "IP block" with "pre-diffused IP block". Claims 1 and 6 have been amended and are believed not objectionable.

Claim Rejections - 35 USC § 102

The Patent Office rejected Claims 1-17 under 35 U.S.C. § 102(e) as being anticipated by Butts et al. (U.S. Patent No. 6,539,535) ("Butts").

Applicant respectfully traverses the rejection. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983). Emphasis added.

Applicant respectfully submits Claims 1-17 recite elements that have not been disclosed by Butts. For example, Claims 1, 6, and 11 generally recite interface pins of at least two pre-diffused IP blocks in a semiconductor device connected to input ports of a multiplexer, connecting an output port of the multiplexer to an I/O pin of the semiconductor device, and connecting the I/O pin to a reusable field programming device so that an IP block having the interface pin is selected for prototyping.

Butts does not disclose interface pins of at least two pre-diffused IP blocks in a semiconductor device connected to input ports of a multiplexer. Butts does not disclose pre-diffused IP blocks. Pre-diffusion refers to a technique where a dopant is deposited onto a wafer prior to a diffusion step. A diffusion step is a process that puts specific amounts of dopant in the wafer surface through openings in the surface layers to create pockets in the wafer surface that are either rich in electrons or electron holes required for operation of the transistors, diodes, capacitors, resistors, and such of the integrated circuit. Customizable circuits include pre-diffused IP blocks which can be utilized by adding final metal layers to customize an integrated circuit. Butts is concerned with a circuit specialized for logic emulation, not customizable integrated circuits. Specialized circuits for logic emulation do not include pre-diffused blocks. Butts does not disclose that any of the blocks are pre-diffused prior to a diffusion step. Thus, Butts does not disclose pre-diffused IP blocks. Therefore, Butts does not disclose interface pins of at least two pre-diffused IP blocks in a semiconductor device connected to input ports of a multiplexer.

Further, Butts does not disclose connecting an output port of the multiplexer to an I/O pin of the semiconductor device and connecting the I/O pin to a reusable field programming device so that an IP block having the interface pin is selected for prototyping. Butts discloses connecting the interface pins of a logic element to a multiplexer within a circuit which is performing the emulation in order to accurately and efficiently emulate logic. The logic element is performing the emulation, it is not selected for prototyping. The circuit of Butts is for a reusable field programming device which could be utilized to prototype a semiconductor device based on hardware emulation, not a semiconductor device being prototyped based on hardware emulation. The multiplexer output port which is connected to an I/O pin in Butts is within a reusable field programming device. It is not a

multiplexer output port which is connected to an I/O pin which is connected to a reusable field programming device. Therefore, Butts does not disclose connecting an output port of the multiplexer to an I/O pin of the semiconductor device and connecting the I/O pin to a reusable field programming device so that an IP block having the interface pin is selected for prototyping.

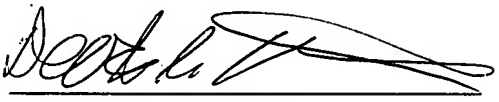
Thus, under *Lindemann*, a *prima facie* case of anticipation has not been established for Claims 1, 6, and 11. Claims 2-5 depend from Claim 1 and are believed allowable due to their dependence upon an allowable base claim. Claims 7-10 depend from Claim 6 and are believed allowable due to their dependence upon an allowable base claim. Claims 12-17 depend from Claim 11 and are believed allowable due to their dependence upon an allowable base claim.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,
LSI Logic, Inc.,

Dated: April 16, 2007

By: 
David S. Atkinson
Reg. No. 56,655

SUITER · SWANTZ PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile